TITLE: APPARATUS HAVING AN INTER-MODULE DATA TRANSFER CONFIRMING FUNCTION, STORAGE CONTROLLING APPARATUS, AND INTERFACE MODULE FOR THE APPARATUS
INVENTORS: Tomoharu MURO
SERIAL NO.:
DOCKET NO.: 1075.1252

FIG. 1

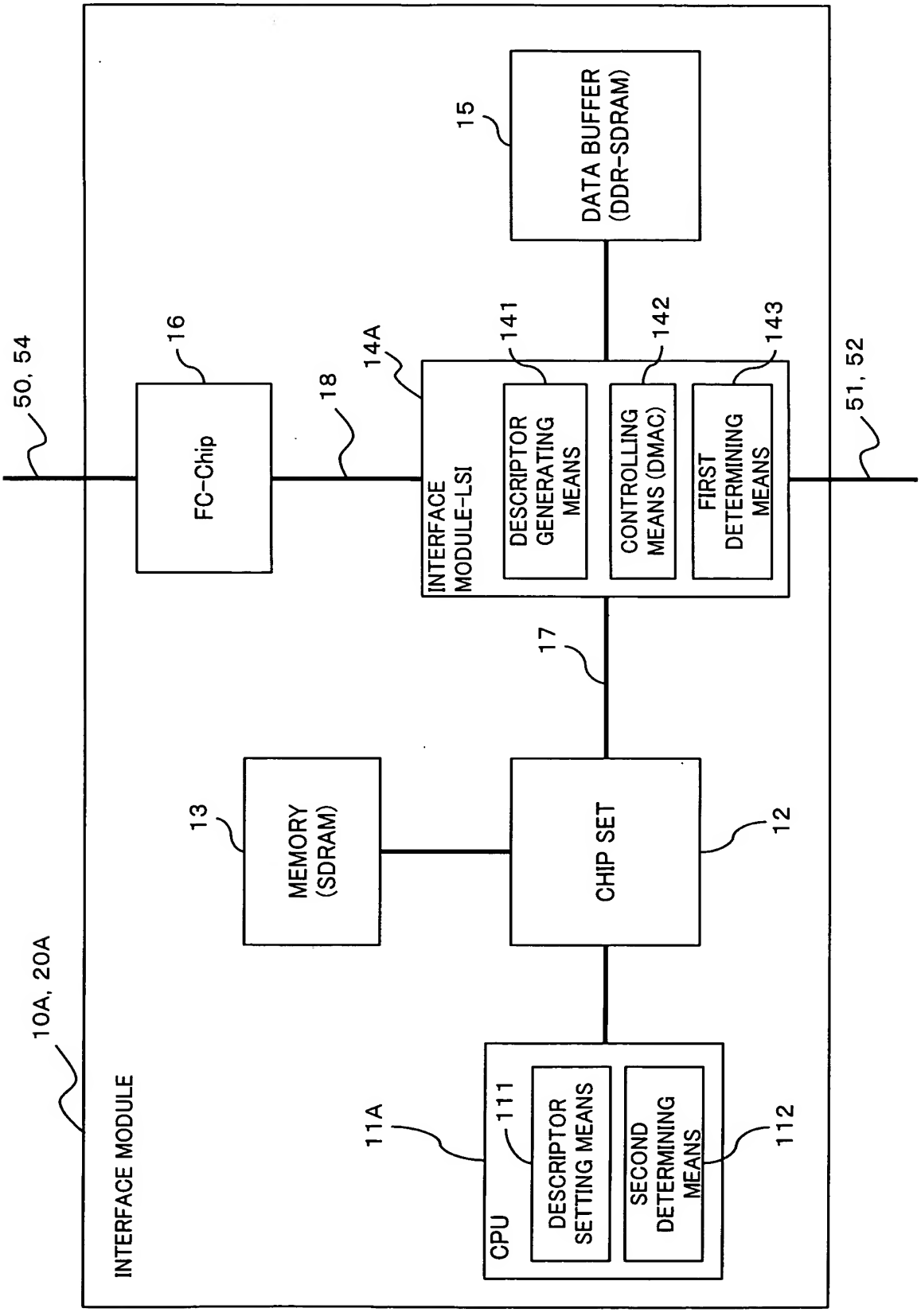

FIG. 2

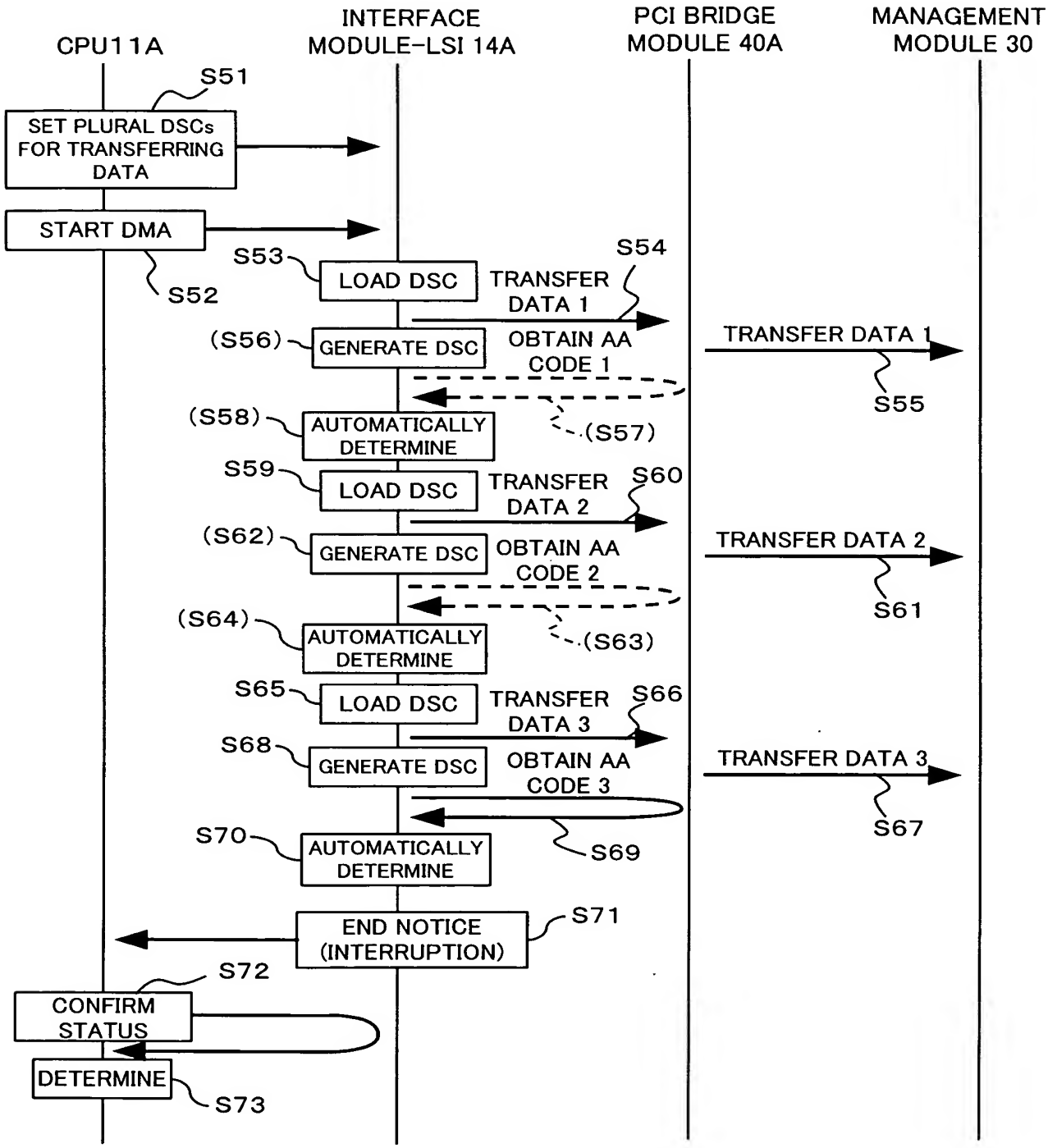
CPU11A
INTERFACE MODULE-LSI 14A
PCI BRIDGE MODULE 40A
MANAGEMENT MODULE 30
S51
SET PLURAL DSCs FOR TRANSFERRING DATA
START DMA
S52
S53
LOAD DSC
TRANSFER DATA 1
S54
(S56)
GENERATE DSC
OBTAIN AA CODE 1
TRANSFER DATA 1
S55
(S57)
(S58)
AUTOMATICALLY DETERMINE
S59
LOAD DSC
TRANSFER DATA 2
S60
(S62)
GENERATE DSC
OBTAIN AA CODE 2
TRANSFER DATA 2
S61
(S63)
(S64)
AUTOMATICALLY DETERMINE
S65
LOAD DSC
TRANSFER DATA 3
S66
S68
GENERATE DSC
OBTAIN AA CODE 3
TRANSFER DATA 3
S67
S69
S70
AUTOMATICALLY DETERMINE
S71
END NOTICE (INTERRUPTION)
S72
CONFIRM STATUS
DETERMINE
S73

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FIG. 3

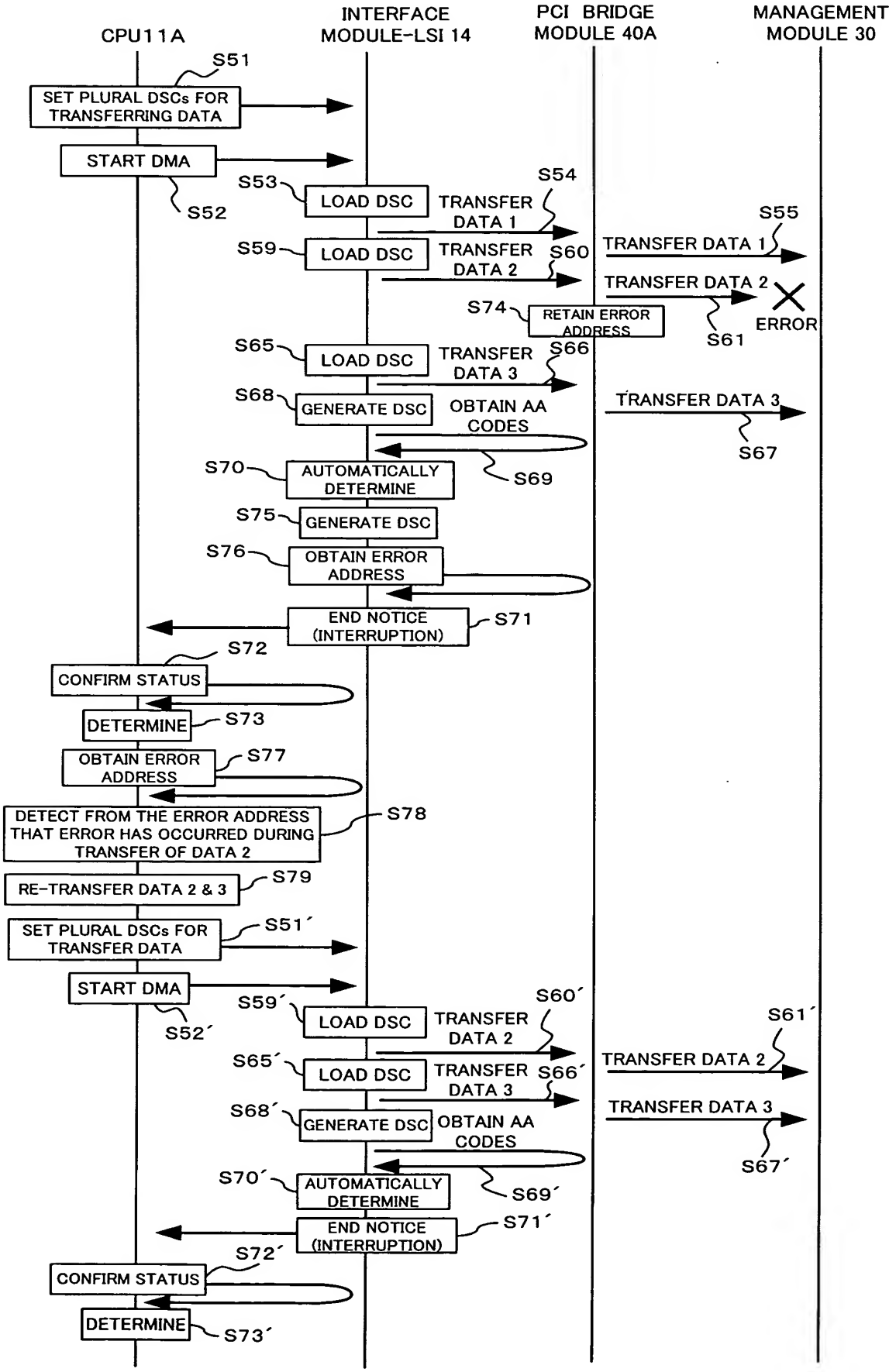


FIG. 4

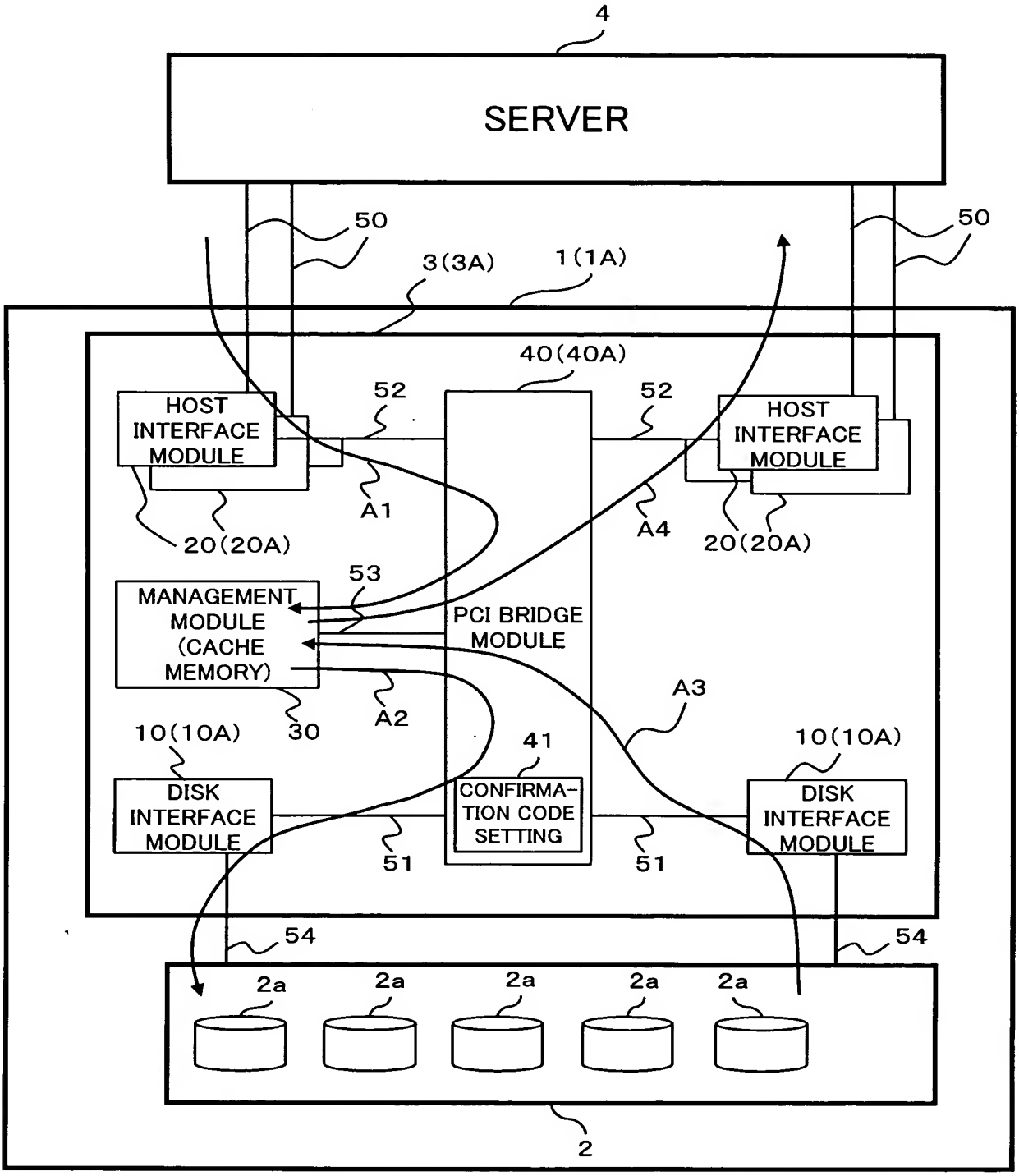
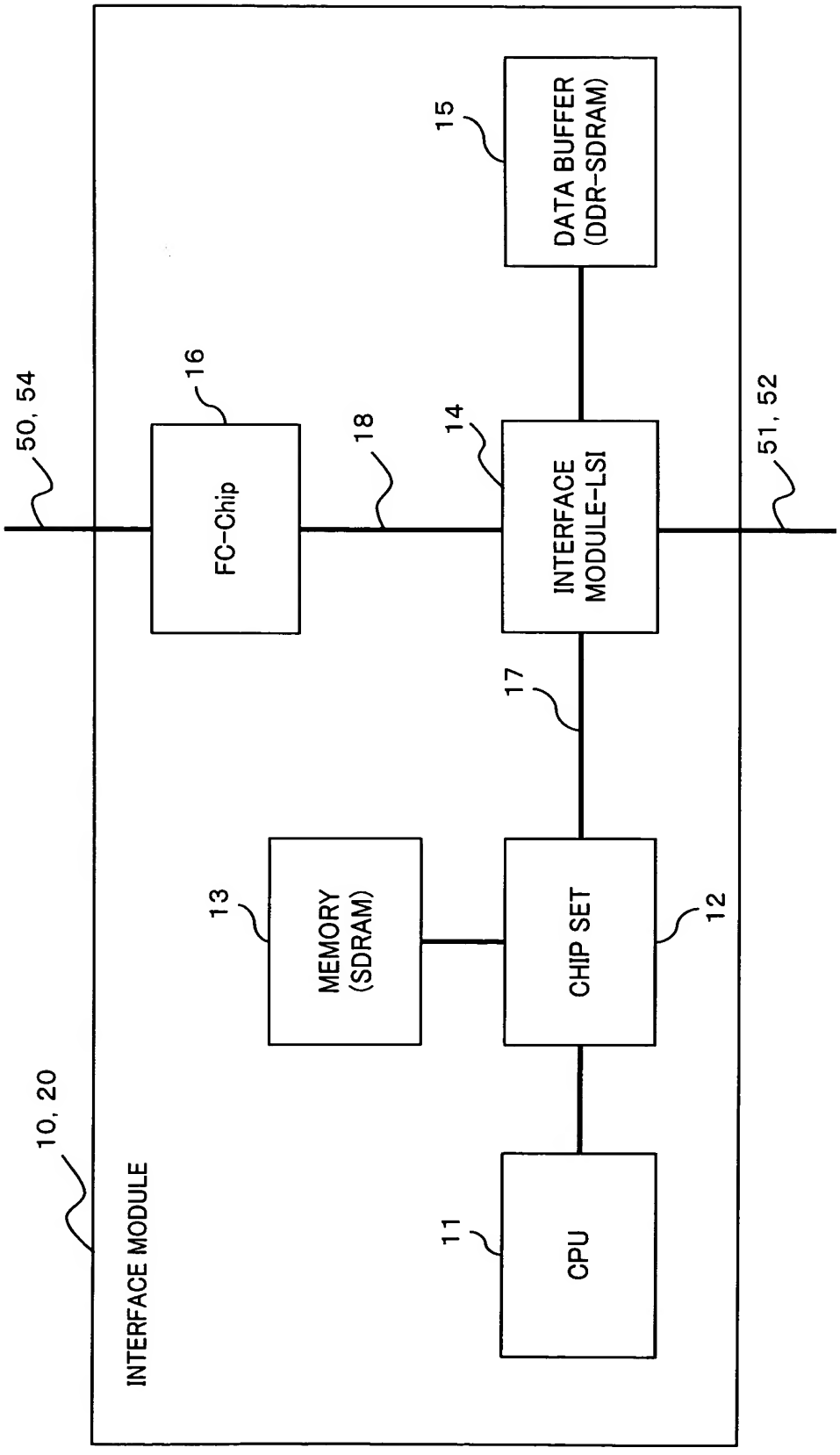

4
SERVER
50
50
3(3A)
1(1A)
40(40A)
52
52
HOST INTERFACE MODULE
HOST INTERFACE MODULE
A1
A4
20(20A)
20(20A)
53
MANAGEMENT MODULE (CACHE MEMORY)
PCI BRIDGE MODULE
A2
30
A3
10(10A)
10(10A)
41
DISK INTERFACE MODULE
CONFIRMATION CODE SETTING
DISK INTERFACE MODULE
51
51
54
54
2a
2a
2a
2a
2a
2

FIG. 5


10, 20
INTERFACE MODULE
CPU
11
CHIP SET
12
MEMORY (SDRAM)
13
INTERFACE MODULE-LSI
14
DATA BUFFER (DDR-SDRAM)
15
FC-Chip
16
17
18
50, 54
51, 52

# FIG. 6
PRIOR ART

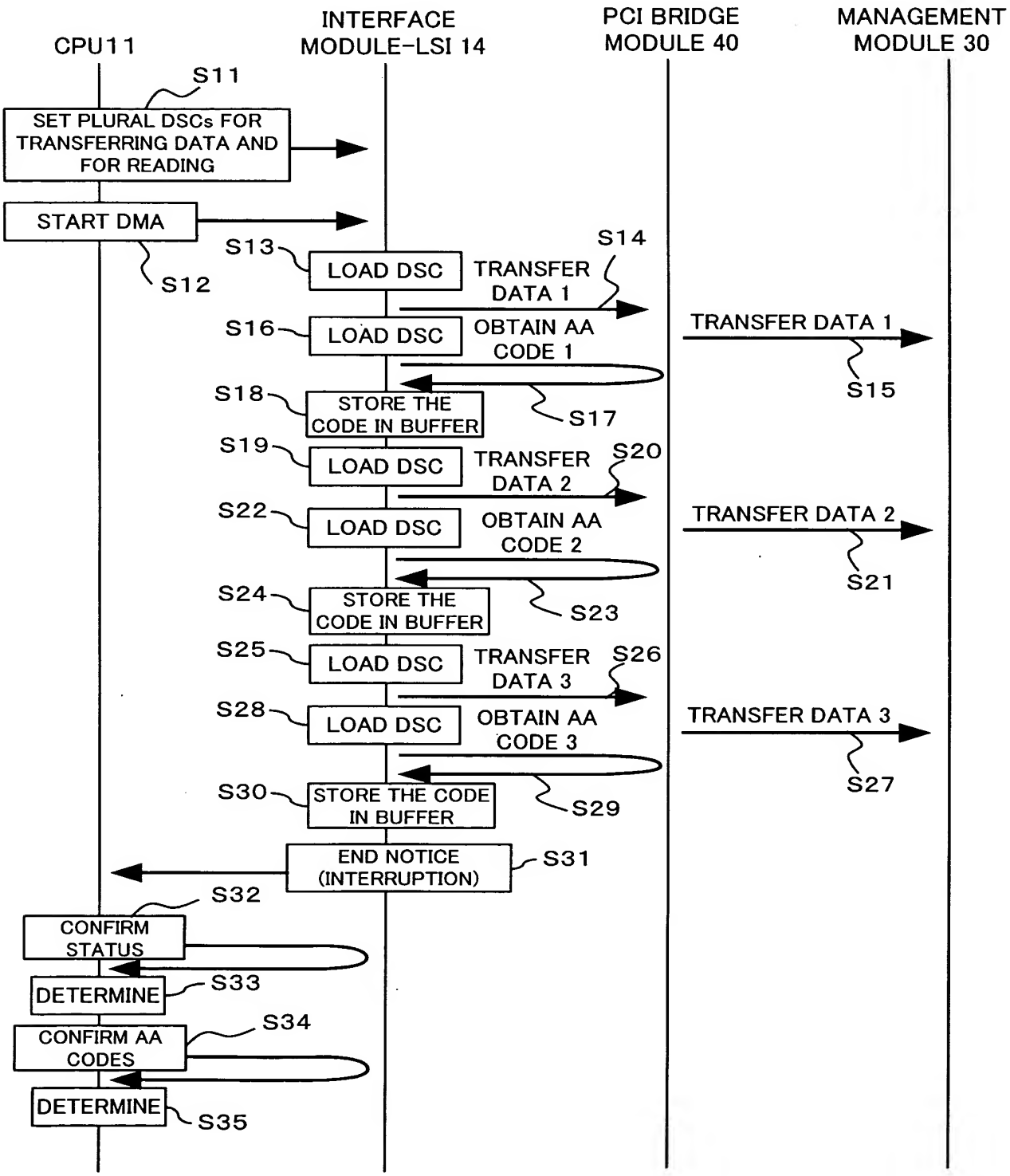


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FIG. 7
PRIOR ART